REMARKS

Claims 1-8 are pending in the present application.

I. FORMAL MATTERS

A. Claim to Priority

Applicant notes with appreciation the Examiner's acknowledgement of the claim to foreign priority under 35 U.S.C. § 119(a)-(d) or (f) and indication that the certified copies of the priority documents have been received.

B. Drawings

The Office Action indicates that the drawings are objected to because Figs. 5, 6 and 7 should be labeled as prior art. Figs. 5, 6 and 7 are described in the subject specification as showing a "conventional" liquid crystal display device (see "Background of the Invention" section and "Brief Description of the Drawings" section of the present application). Therefore, Figs. 5, 6 and 7 are not "prior art" under 35 U.S.C. § 102. Thus, Applicant submits that the Examiner's requirement to designate Figures 5, 6 and 7as "Prior Art" is improper. Accordingly, Applicants has not labeled Figures 5, 6 and 7 as "Prior Art."

C. Rejection of Claim 8 Under 35 U.S.C. 112, First and Second Paragraphs

Claim 8 is rejected under 35 U.S.C. § 112, first and second paragraphs, as allegedly not complying with the enablement requirement and not being definite. The Examiner asserts that the limitation "signal circuit" is not described in the specification and therefore is not clear. Also, the Examiner asserts that he does not understand whether the signal circuit is a circuit with an input signal or an output signal.

Applicant has amended herein the "signal circuit" of claim 8 to "timing signal generation circuit," as shown above. The "timing signal generation circuit" is described clearly on page 37, line 17 through page 38, line 12. Also, has made a very minor amendment to claim 5, as shown above.

II. PRIOR ART REJECTION

Claims 1-8 are rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 6,211,849 (Sasaki). This rejection is traversed.

The Examiner asserts that Sasaki teaches all of the features of claim 1 including a plurality of column and row electrodes connected in series, a data input section, a control logic section, a shift register circuit and a data output section.

Applicant submits that Sasaki does not teach or suggest the "selection section" of independent claim 1. The Examiner fails to mention this claim feature is his rejection.

Regarding independent claim 5, Applicant submits that Sasaki does not teach a control data signal that is input to a first column electrode driving circuit that is closest to the row electrode driving circuits. The Examiner does not mention this claim feature in his rejection.

Regarding independent claim 6, Applicant submits that Sasaki does not teach or suggest a timing signal output from a first column electrode driving circuit that is supplied to a first row electrode driving circuit. The sections of Sasaki relied on by the Examiner, Figs. 4 and 13, do not appear to show this feature. Rather, Fig. 4 merely shows the clock line CLK being input from one row/column electrode driving circuit to the next row/column electrode driving circuit.

Regarding independent claim 7, Applicant submits that Sasaki does not teach or suggest a timing signal for controlling the plurality of row electrode driving circuits that is supplied to a row electrode driving circuit sequentially through a second line portion provided on the printed circuit board, a third line portion provided on one of the plurality of column electrode driving circuits, and a fourth line portion provided on the display panel. The Examiner asserts that this feature of claim 7 is disclosed in Figs. 4 and 13 of Sasaki. Applicant submits that Figs. 4 and 13 of Sasaki only show

the row or column drivers, and do not disclose the plurality of line portions extending from a column electrode driving circuit to a row electrode driving circuit of claim 7.

Regarding independent claim 8, Applicant submits that Sasaki does not teach or suggest a first column electrode that generates a timing signal for controlling a plurality of column electrode driving circuits and a plurality of row electrode driving circuits. The Examiner does not mention this feature in his rejection. The Examiner only mentions that Sasaki allegedly teaches a timing signal that is output from one column electrode driving circuit to the next column electrode driving circuit.

Sasaki discloses a liquid crystal display device composed of a plurality of scanning lines formed along rows of the liquid crystal pixels, and a plurality of signal lines formed along columns of the liquid crystal pixels, and a display control circuit for selecting a row of the liquid crystal pixels via each of the scanning lines and controlling voltages across the liquid crystal pixels of the selected row via the signal lines (See abstract).

The Examiner asserts that Sasaki teaches "a selection section for selecting one of a signal in synchronization with the timing signal generated by the timing control section *and* the control data signal input to the data input section, *based on the* control *data* signal input to the data input section" as recited in pending claim 1. Applicant submits that Sasaki does not teach or suggest the above feature as recited in pending claim 1. Specifically, as clearly shown in Figure 4 of Sasaki, all the *inputs,* (CLK for transmitting the clock signal, DATA for transmitting the pixel data signal and CNT for

transmitting the control signals) via the input pad portion 2, are output from the output pad portion 3 to the next driver IC 1 (see , column 4, line 36-42).

Therefore, Applicant submits that the Examiner has not demonstrated that Sasaki discloses the "selection section" of claim 1.

Further, Applicant submits that Sasaki does not teach or suggest "a timing signal for controlling an operation timing of the plurality of column electrode driving circuits and the plurality of row electrode driving circuits is generated in the first column electrode driving circuit ...," as recited in claim 5. Rather, Sasaki discloses an interface unit 25 for entering a power voltage, a pixel date signal, a clock signal and other control signals, supplied from an external liquid crystal controller, a *scanning* line driver 24 for receiving the power voltage and the control signals from the interface unit 25 ... and includes a pair of signal line 23 for receiving the power voltage, the pixel data signal, the clock signal and the control signals entered by the interface unit 25 to perform at the power voltage ... (see column 4, line 3-18). Additionally, Figure 3 of Sasaki merely discloses that the driver ICs are connected in cascade by inter-module wirings 10 ... each driver IC 1 receives these signals via *an* input pad *portion* 2 sequentially supplies the pixel data signal ... to be output from its output pad portion 3 to the next driver IC 1 (see column 4, line 28-45).

Therefore, Sasaki does not disclose a timing signal for controlling an operation

timing of the plurality of column electrode driving circuits and the plurality of row electrode driving circuits is generated in the first column electrode driving circuit. Furthermore, Sasaki does not disclose, "the generated timing signal is transferred in a cascading manner to the plurality of row electrode driving circuits as a scanning signal" as recited in claim 5.

Similarly, claim 6 has the same distinguishing features as discussed above in regards to claim 5. Thus, claim 6 also is not anticipated by Sasaki.

Therefore, because Sasaki does not teach each and every feature of independent claims 1, 5, 6, 7 and 8, Sasaki does not anticipate claims 1-8. Thus, the rejection of claims 1-8 under 35 U.S.C. § 102(b) is improper and should be withdrawn.

If the Examiner believes that any of the outstanding issues could be resolved by a telephone interview, the Examiner is kindly invited to call the undersigned at the listed telephone number.

Applicant believes that no additional fees are due for the subject application. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,

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